REMARKS

This amendment responds to the Final Office Action mailed July 9, 2007. In the office action the Examiner:

- objected to the specification for informalities;
- objected to the drawings;
- objected to claims 6 and 27 for informalities;
- rejected claims 1-42 as being indefinite under 35 U.S.C. 112, second paragraph;
- rejected claims 1-4, 21-26 and 42 under 35 U.S.C. 102(e) as being anticipated by Desai (US 6,862,296); and
- rejected claims 5, 13, 14, 18-20, 34, 35 and 39-41 under 35 U.S.C. 103(a) as being unpatentable over Desai (US 6,862,296).

After entry of this amendment, the pending claims are: claims 1-42.

CLAIM AMENDMENTS

Claims 1, 2, 8, 9, 14, 15, 21, 27, 29 and 35 have been amended. No new matter has been added as a result of these amendments. Support for the amendments to claims 21, 29 and 35 can be found at least in the claims as originally filed, and in paragraph 0032 of the specification, as originally filed. Support for the amendments to claim 27 can be found at least in the claims as originally filed, and in Figs. 2C and 2D and in paragraph 0038 of the specification as originally filed.

It is noted that the amendments to claims 1, 2, 8, 9, 14, and 15 do not change the scope of those claims, and are made solely for clarification. For instance, the "detecting a duty cycle" operation in claim 1 detects the duty cycle of a data signal, and therefore the addition of " of the data signal" to the "comparing" operation in claim 1 does not change the scope of claim 1.

AMENDMENTS TO THE SPECIFICATION

The Specification has been amended to correct typographical errors. No new matter has been added as a result of these amendments.

REMARKS CONCERNING REVISED FIGURES

Revised Figures 1A and 1B are included in Appendix A. Figures 1A and 1B have been amended to remove the "Prior Art" label. Applicant respectfully submits that Figures

1A and 1B are not prior art and were erroneously labeled as such. Applicant respectfully points the Examiner to Paragraph 0025 of the originally filed specification, which states that "FIG. 1 illustrates a simplified system for data transmission using an adjustable receiving duty cycle circuit according to one embodiment of the present invention."

The Examiner is respectfully requested to approve the proposed drawing changes.

OBJECTIONS TO THE SPECIFICATION

The Examiner objected to the specification stating that there is no predetermined duty cycle signal input to duty cycle detector circuit 228. Applicant respectfully submits that it is not required that the predetermined duty cycle signal be inputted to duty cycle detector circuit 228. A person of ordinary skill in the art would recognize that other alternatives exist. For example, the predetermined duty cycle signal can be stored in a storage element, such as a register, on the duty cycle detector circuit 228. Alternatively, or in addition, the predetermined duty cycle signal can be pre-programmed in the duty cycle detector circuit 228. Also, for at least some predetermined duty cycles, such as a 50% duty cycle, there is no need for an input of the predetermined duty cycle because the predetermined duty cycle is determined by circuitry internal to the duty cycle detector or duty cycle adjuster, depending on the embodiment. Therefore, Applicant respectfully submits that no correction to the specification is required.

37 C.F.R. § 1.83(a) OBJECTIONS

The following information and remarks are provided solely for the purpose of identifying exemplary portions of the specification that meet the requirements of 35 Rule 1.83(a) with respect to pending claims 21 and 27. The remarks are not directed to the scope of the pending claims, and are not to be construed as limiting the scope of the pending claims.

The Examiner has objected to the figures for not showing the "first correction circuit" of claim 21 and "second correction circuit" of claim 27. Applicant has amended claims 21 and 27, such that they no longer recite a "first correction circuit" and a "second correction circuit" respectively. Further, Applicant respectfully submits that support for the newly added language of "one or more circuits", can be found at least in Figure 2A, which illustrates a "Clock Duty Cycle Adjuster 214," and Figure 2C, which shows another embodiment of a circuit that includes a "Clock Duty Cycle Adjuster 214." Further, paragraph 0032 of the specification states:

> Additionally, some embodiments include an analog-to-digital converter to convert analog signals from the duty cycle detector 208 into digital values that can be used by the *duty cycle correction circuits within the clock duty cycle adjuster 214*. Further embodiments include a comparator to determine a difference between the detected duty cycle and the predetermined duty cycle. The difference is then used by the *duty cycle correction circuits in the clock duty cycle adjuster 214* to correct the receiver clock duty cycle to match the duty cycle of the predetermined duty cycle.

(Emphasis Added).

CLAIM OBJECTIONS

The Examiner objected to claims 6 and 27, and associated dependent claims 7-11 and 28-32, stating that no drawing shows a second correction circuit configured to adjust the duty cycle of the receiver clock signal in accordance with a third difference between the detected system clock signal duty cycle and the predetermined duty cycle.

Applicant respectfully submits that support in the drawings for claims 6 and 27 can be found at least in Figures 2C and 2D. Figure 2C illustrates a "Duty Cycle Detector 208" and a "Clock Duty Cycle Adjuster 214." As shown in Figure 2C, "Duty Cycle Detector 208" receives a buffered system clock input and outputs duty cycle correction (DCC) values 210 and 212. Clock Duty Cycle Adjuster 214 receives the DCC values 210 and 212 and skew values (SkA 216 and SkB 218). Figure 2D illustrates an embodiment of a duty cycle detector. Further, corresponding to Figure 2D, Paragraph 0038 of the originally filed specification states:

> The common mode detector 252 outputs a signal 253 that equals or represents the average voltage level of the input signal 251 to the detector 252. The input signal may be either a clock signal or a data signal. The output signal 253 is compared with a reference voltage 256 (or other appropriate reference signal) by a comparator 254.... *The difference between the common mode voltage of the input signal and a reference voltage is indicative of the difference between the duty cycle of the input signal and a predefined duty cycle.* (Emphasis Added).

CLAIM REJECTIONS – 35 U.S.C. § 112

The Examiner rejected claims 1-42 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following remarks, addressing the rejections under 35 U.S.C. § 112, second paragraph, are directed to specification support for claim elements and clarity of the claim limitations, and are not directed to the scope of these claim elements.

Claim 1

Applicant respectfully submits that support for the claim limitations of "detecting a duty cycle of a data signal," and "comparing the detected duty cycle with a predetermined duty cycle in order to determine a first difference between the detected data signal duty cycle and the predetermined duty cycle," can be found at least in Figures 2B and 2D.

Figure 2B illustrates a "Duty Cycle Detector 208" that receives a data signal 226. Figure 2D illustrates an embodiment of a duty cycle detector. Further, corresponding to Figure 2D, Paragraph 0038 of the originally filed specification states:

> The common mode detector 252 outputs a signal 253 that equals or represents the average voltage level of the input signal 251 to the detector 252. The input signal may be either a clock signal or a data signal. The output signal 253 is compared with a reference voltage 256 (or other appropriate reference signal) by a comparator 254.... *The difference between the common mode voltage of the input signal and a reference voltage is indicative of the difference between the duty cycle of the input signal and a predefined duty cycle.* (Emphasis Added).

Claim 2

Applicant respectfully submits that support for the claim limitations of "comparing the detected duty cycle with a predetermined duty cycle comprises comparing the first duty cycle with a first predetermined duty cycle in order to determine a first difference between the first duty cycle and the first predetermined duty cycle, and comparing the second duty cycle with a second predetermined duty cycle in order to determine a second difference between the second duty cycle and the second predetermined duty cycle," can be found at least in paragraph 0036 of the originally filed specification, which states:

> Still referring to FIGS. 2A and 2B, in some embodiments the device in which the receiver clock circuitry of FIGS. 2A and 2B resides receives data signals from first and second devices.... During calibration a first adjustment value (e.g., comprising a first set of skew values) will be determined by comparing the duty cycle of the data signal from the first device with a first predetermined duty cycle, and a second adjustment value (e.g., comprising a second set of skew values) will be determined by comparing the duty cycle of

the data signal from the second device with a second predetermined duty cycle.

Claim 6

Applicant respectfully submits that support for the claim limitations of "comparing the duty cycle of the system clock signal with the predetermined duty cycle," can be found at least in Figures 2C and 2D.

Figure 2C illustrates a "Duty Cycle Detector 208" that receives a buffered clock signal 204. Figure 2D illustrates an embodiment of a duty cycle detector. Further, corresponding to Figure 2D, Paragraph 0038 of the originally filed specification states:

> The common mode detector 252 outputs a signal 253 that equals or represents the average voltage level of the input signal 251 to the detector 252. The input signal may be either a clock signal or a data signal. The output signal 253 is compared with a reference voltage 256 (or other appropriate reference signal) by a comparator 254.... *The difference between the common mode voltage of the input signal and a reference voltage is indicative of the difference between the duty cycle of the input signal and a predefined duty cycle.* (Emphasis Added).

Claim 21

Applicant respectfully submits that support for the claim limitations of "data signal duty cycle detector configured to detect a first duty cycle of a first data signal and to generate a first difference signal representing a difference between the first duty cycle and a first predetermined duty cycle," can be found at least in paragraph 0038 of the originally filed specification and Figures 2B and 2D.

Figure 2B illustrates a "Duty Cycle Detector 208" that receives a data signal 226. Figure 2D illustrates an embodiment of a duty cycle detector. Further, corresponding to Figure 2D, Paragraph 0038 of the originally filed specification states:

> The common mode detector 252 outputs a signal 253 that equals or represents the average voltage level of the input signal 251 to the detector 252. The input signal may be either a clock signal or a data signal. The output signal 253 is compared with a reference voltage 256 (or other appropriate reference signal) by a comparator 254.... *The difference between the common mode voltage of the input signal and a reference voltage is indicative of the difference between the duty cycle of the input signal and a predefined duty cycle.* (Emphasis Added).

Accordingly, favorable reconsideration and withdrawal of the rejection of claims 1, 2, 6, 21 and associated dependent claims 3-5, 7-20 and 22-41 under the first paragraph of 35 U.S.C. §112 are respectfully requested.

CLAIM REJECTIONS – 35 U.S.C. § 102

The Examiner rejected claims 1-4, 21-26, 34, 35, and 42 under 35 U.S.C. § 102(e) in view of Figure 5 of Desai. For a proper showing that Desai anticipates these claims, Desai must disclose all elements of each rejected claim. Furthermore, the "broadest reasonable interpretation" of the claim limitations must be consistent the plain and ordinary meaning of the claim terms, and must not be inconsistent with the way the claim terms are used in the specification, per MPEP 2111 and MPEP 2111.01.III. As discussed in more detail below, the Examiner's interpretation of "duty cycle" and "detecting a duty cycle of a data signal" are inconsistent with the plain and ordinary meaning of the term "duty cycle," which has a well established meaning in the arts of circuit design and signal processing.

The rejected claims include independent claims 1, 21 and 42.

Claims 1-4

With respect to independent claim 1, as amended, Applicant respectfully submits that Desai does not teach or suggest "comparing the detected duty cycle with a predetermined duty cycle in order to determine a first difference between the detected data signal duty cycle and the predetermined duty cycle," as claimed. As explained in more detail below, the retiming function of sampling flip-flop 502 inherently prevents any downstream circuitry in Desai from detecting or evaluating the duty cycle of the received data signal, because the retiming function of the sampling flip-flop destroys the timing information that would be needed to detect or evaluate the duty cycle of the data signal.

Desai discloses a comparator 508. However, comparator 508 does not detect and compare duty cycles. In fact, the comparator 508 cannot receive any information concerning the duty cycle of the received serial data, because the sampling flip-flop 502 "retimes the serial data." (Desai, Col. 3, lines 46-47). Thus, no information about the duty cycle of the received data can propagate beyond the sampling flip-flop 502, making it impossible for any later circuit to detect the duty cycle. Furthermore, the reference pattern is a predetermined series of bits, not a predetermined duty cycle.

The Examiner states that Desai's comparator "detects the high level of the data signal (serial data) and provides an output signal that [reflects] the high level (and the low level) of

the data signal" and is therefore a duty cycle detector. (Office Action dated 07/09/07, p. 8). The Examiner cannot arbitrarily assign a term of art another meaning that is contrary to its standard usage in the field. *See* MPEP 2111.01.III ("The ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.).

Applicant respectfully submits that the phrase "duty cycle" is a term of art having a specific meaning in the field of electrical engineering. It is well known in the field of electrical engineering that "duty cycle" is a measure of a percentage of time. Specifically, in the field of electronic circuits, the term "duty cycle" is the ratio of on time to cycle time. See, e.g., Federal Standard 1037C: Glossary of Telecommunications Terms, published August 7, 1996, which defines "duty cycle" as "in a periodic phenomenon, the ratio of the duration of the phenomenon in a given period to the period." (A dictionary print-out is attached herewith as Appendix B for the Examiner's reference.)

Therefore, Applicant respectfully submits that Desai does not teach or suggest "comparing the detected duty cycle with a predetermined duty cycle in order to determine a first difference between the detected data signal duty cycle and the predetermined duty cycle," as claimed. Because, Desai does not teach or suggest each and every limitation of claim 1, it does not anticipate claim 1 and associated dependent claims 2-4.

Claims 21-26, 34, 35

With respect to independent claim 21, Applicant respectfully submits that Desai does not teach or suggest "a data signal duty cycle detector configured to detect a first duty cycle of a first data signal," as recited in claim 21.

As discussed above, with reference to claim 1, Desai's comparator 508 does not detect and compare duty cycles. Therefore, Desai's comparator 508 does not "a data signal duty cycle detector configured to detect a first duty cycle of a first data signal," as recited in claim 21.

Because, Desai does not teach or suggest each and every limitation of claim 21, it does not anticipate claim 21 and associated dependent claims 22-26, 34 and 35.

Claim 42

With respect to independent claim 42, Applicant respectfully submits that Desai does not teach or suggest circuitry to "detecting a duty cycle of a data signal and for generating a first difference signal representing a difference between the detected data signal duty cycle

and a predetermined duty cycle," at least for the same reasons as those for claim 1, as discussed above.

Because, Desai does not teach or suggest each and every limitation of claim 42, it does not anticipate claim 42.

CLAIM REJECTIONS – 35 U.S.C. § 103

The Examiner rejected claims 5, 13, 14, 18-20, and 39-41 under 35 U.S.C. § 103(a) in view of Figure 5 of Desai. These claims all depend on either claim 1 or claim 21. As discussed above, the rejection of independent claims 1 and 21 in view of Desai should be withdrawn. Therefore, these claims (5, 13, 14, 18-20, and 39-41) are patentable over Desai for at least the same reasons as claims 1 and 21.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

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Appendix A

Revised Figures (see attached copies)